Course: ECE 27000 - Introduction to Digital System Design

Type of Course: Required for CmpE and EE Programs

Catalog Description: An introduction to digital system design and hardware engineering, with an emphasis on practical design techniques and circuit implementation.

Credits: 4

Contact Hours: Class:3, Lab: 3

Corequisite: ENGR 12800

Prerequisites by Topics: Basic understanding of circuits (voltage, current, Ohm's Law) and electrical components (resistors, capacitors, switches).


Course Objectives: This course will provide a comprehensive understanding of the principles and practices of digital logic circuits. Students should be able to analyze, design and implement combinational and sequential circuits.

The laboratory sessions form an integral part to provide practical experiences in hardware and software analysis and design.

Course Outcomes: Students who successfully complete this course will have demonstrated:

1. An ability to analyze and design combinational logic circuits. (a, c, e, k)
2. An ability to analyze and design synchronous sequential state machines. (a, c, e, k)
3. An ability to realize digital circuits using programmable logic devices. (c, k)
4. An ability to perform arithmetic operations on signed binary numbers and build digital circuits that implement arithmetic functions. (a, c, e, k)
5. An ability to incorporate different building blocks (decoders, multiplexers, encoders, registers, etc.) in the design of a digital system. \( \text{a, b, c, e, k} \)
6. An ability to present lab results effectively in forms of lab reports. \( \text{g} \)

**Lecture Topics**

1. Number systems and codes
2. Digital electronic signals and switches
3. Basic logic gates
4. Programmable Logic Device: Xilinx CPLDs and FPGAs
5. Boolean Algebra
6. Exclusive-OR and Exclusive-NOR Gates
7. Arithmetic operations and circuits
8. Code converter, multiplexers, and demultiplexers
9. Logic families and their characteristics
10. Flip-flops and registers
11. Practical considerations for digital design
12. Counter circuits and sequential state machine
13. Shift registers

**Computer Usage**

High

**Laboratory Experience**

High

**Design Experience**

High

**Coordinator**

Chao Chen, Ph.D.

**Date**

03/02/2018